Optimum Phase-Acquisition Technique for Charge-Pump PLL

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***Abstract*— In this paper, we propose a new optimum phase-acquisition algorithm controlling the loop gain of a charge-pump PLL (CP-PLL) in the sense of the MMSE criterion. A set of recursive difference equations minimizing rms jitter of output phase is derived to obtain an optimum gear-shifting sequence with a zero-phase start (ZPS) assumption. It is shown that the optimum gear-shifting sequence is independent of the variance of the input phase jitter. A procedure for applying this sequence to the design of CP-PLL circuits is described. Both behavioral simulation and HSPICE circuit-level simulation demonstrate that the proposed design leads to an efficient CP-PLL having both fast acquisition and significant jitter reduction characteristics. The optimal gear-shifting CP-PLL outperforms the conventional CP-PLL's. These methods can be used for clock recovery applications such as data communication receivers, disk drive read/write channels, and local area networks, as well as for other applications requiring very short initial preamble periods.**

***Index Terms*— Charge–pump PLL (CP–PLL), gear-shifting, MMSE criterion, optimum sequence, phase-acquisition, zero-phase start (ZPS).**

I. Introduction

THERE has been increasing demand for high speed and low noise data receivers such as data communication receivers, disk drive read/write channels, and high speed modems, etc. In such applications, clock recovery is required to show better performance for the extraction of timing from incoming data [1]–[4].

Of various techniques, such as the LC-tank circuit, the surface acoustic wave (SAW) filter, the X-tal filter, and the PLL, the PLL is one of the most desirable components for timing extraction because of its low cost, high integration, and easy and wide availability [5].

The PLL incorporating the sequential-logic phase-frequency detector (PFD) has been widely used in recent years because of its extended tracking range, frequency sensitive error signal, and low cost availability in integrated circuit chips. The logic states of the PFD are converted into analog quantity by using a charge pump and passed through the loop filter (LF). The LF output controls the voltage-controlled oscillator (VCO) of the PLL. The charge-pump PLL (CP-PLL) is known to be capable of tracking the input phase extremely accurately [6]–[9].

In clock recovery applications, there have been efforts to analyze and design a desirable PLL having a fast locking characteristic and low jitter [10]–[15]. In such applications, however, those two requirements (fast locking and sufficiently small phase jitter) cannot be met simultaneously using a conventional PLL design. A common approach to overcoming this difficulty is to design a narrow-band loop to meet the phase jitter requirement, and to enhance locking speed by using such forms of acquisition aiding techniques as:

- zero-phase start (ZPS);
- switching of the loop filter;
- switching of the loop gain;
- new phase comparator with/without frequency detector.

The first is generally used in implementations of recent integrated data separators and synchronizers [2], [3], [16]–[18]. It is aimed at minimizing the initial phase step and thus resulting in a reduced phase acquisition time by starting VCO in a precise, controlled phase with respect to the incoming clock or data [19]. Although it improves the acquisition speed significantly, it requires additional long frequency training period with a local clock generator before the ZPS operation starts. In the second, a loop filter with a large bandwidth is used during the acquisition process, and then switched to a narrow bandwidth after lock is achieved [20], [21]. This method requires lock detector to control the switch [22]. The third method is reported in recent digital PLL designs [2], [3], [23]–[25]. A method used in disk drive read channel devices employs two charge pump circuits to provide a high-gain mode for fast phase acquisition and a low-gain mode for phase tracking after synchronization is achieved [16]. However, obtaining good estimation of the input frequency still requires a long training period. The two-mode pull-in technique based on varying the damping factor of PLL combines the second and the third methods [26], but it cannot significantly reduce locking time. In recent years, much improvement has been made in the fourth method [27]–[29]. Shirahama *et al.* [29] used a frequency difference detector (FDD), a modified phase comparator (PC), a smoothing filter (SF) and some additional control circuits. They reduced the pull-in time by 1/10 over the conventional method while maintaining low output jitter. The FDD in this PLL system uses both the rising and falling edges of the input signal, enabling even the detection of Non-Return-to-Zero (NRZ) input signal using its double-sampling effect. Most of these have been based on heuristic or empirical methods, and their automatic mode switchings have not been fully investigated.

This paper proposes a salient phase-acquisition algorithm controlling the PLL loop gain, thereby achieving both fast frequency-phase acquisition and significant jitter reduction.

Manuscript received June 2, 1995; revised March 12, 1996. This paper was recommended by Associate Editor K. Nagaraj.

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Publisher Item Identifier S 1057-7130(97)06033-3.

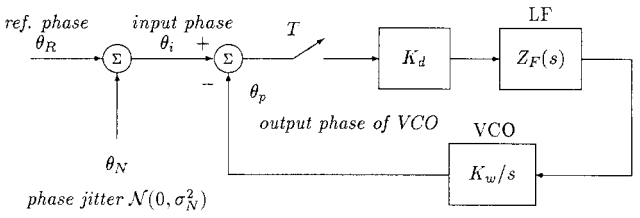


Fig. 1. Linearized model of CP-PLL where K_d is the gain of the phase frequency detector (PFD), $Z_F(s)$ is the loop filter transfer function, and K_w is the VCO gain.

A procedure for applying this algorithm to the design of PLL circuits will also be developed. The proposed algorithm minimizes the mean-squared error (MSE) of PLL output phase jitter, which simultaneously maximizes locking speed and eventually leads to the steady-state. A set of difference equations is derived to obtain the optimum gear-shifting sequence under the minimum mean-square error (MMSE) criterion. The optimum sequence is generated based on the ZPS assumption and used in implementing a gear-shifting circuit of a CP-PLL. Algorithmic simulation results show that the proposed gear-shifting algorithm outperforms conventional CP-PLL's. Charge-pump current values corresponding to the optimum gear-shifting sequence are used as control parameters adjusting the loop gain in the new CP-PLL system since it is generally difficult to change the value of filter components such as loop capacitors or loop resistors. HSPICE circuit simulation results are presented to verify the performance of the gear-shifting CP-PLL. The algorithm can be used for carrier recovery or clock recovery in mobile communications, local area networks, and disk drive read/write channel, etc. which require very short initial preamble periods.

In Section II, an optimum phase-acquisition algorithm generating the optimum gear-shifting sequence for a CP-PLL is described. Behavioral simulation results are presented, along with some comparison with the conventional CP-PLL of fixed control parameters. Section III explains a procedure for applying the algorithm to the design of CP-PLL circuits with PLL circuit-level modeling. Stability limit considerations are also provided. Circuit simulation results using HSPICE are provided to verify the designed CP-PLL performance. Finally, Section IV gives some concluding remarks.

II. Optimal Gear-Shifting Algorithm for PLL

In this section, we derive a phase-acquisition algorithm minimizing a preamble period, i.e., maximizing CP-PLL locking speed while maintaining low jitter output in the steady-state. An optimum gear-shifting loop gain sequence is generated by the algorithm, and applied to the gain control of the linearized PLL model. The superiority of the algorithm over the conventional CP-PLL is verified through behavioral simulation.

A. Generation of the Optimum Gear-Shifting Sequence

We use a PLL to extract an exact clock and/or data timing. For this purpose, a PLL makes an attempt to reduce a output *phase jitter*, which is a phase difference between the VCO output, and the true reference component of the external input signal [30]. To reach this goal, we take an rms phase jitter as a cost function which is defined as the MSE between the true phase and the VCO output phase. This cost function is minimized at each sampling time of a charge-pump circuit. A CP-PLL is modeled as a linearized discrete-time system, since the PFD and charge-pump circuit operate as a discrete-time system. Of various linearized PLL modelings which have been accomplished by several authors [23], [31], we will use the linearized model in [23], which is shown in Fig. 1, since the one in [31] is valid only when the phase tracking errors are small. In Fig. 1, the input phase jitter is a noise source added to the input clock phase. By using this model, the MSE will be defined and minimized to derive a phase-acquisition algorithm.

The transfer function of the output phase $\Theta_p(z)$, in terms of the input phase $\Theta_i(z)$, is derived by applying the impulse-invariant transformation to $\Theta_p(s)/\Theta_i(s)$[1] and represented by

$$\frac{\Theta_p(z)}{\Theta_i(z)} = \frac{K_d K_w Z_F'(z) z^{-1}}{1 + K_d K_w Z_F'(z) z^{-1}} \tag{1}$$

where

$$Z_F'(z) = T \cdot \mathcal{Z}\left\{ \mathcal{L}^{-1}\left[\frac{Z_F(s)}{s} \right]_{t=kT} \right\}.$$

Here K_d and K_w are the phase detector gain given by $I_p/2\pi$ and the VCO gain given by df/dv, respectively, and $Z_F'(z)$ is the z-transform of the *sampled version* of $Z_F(s)/s$, where $Z_F(s)$ is the transfer function of the PLL loop filter in s-domain. $\mathcal{L}^{-1}$ denotes the inverse Laplace transform. If the loop filter is assumed to be a lead-lag filter composed of a resistor R in series with a capacitor C, i.e., $Z_F(s) = R + 1/sC$, then (1) becomes

$$\frac{\Theta_p(z)}{\Theta_i(z)} = \frac{Kz^{-1} - K\beta z^{-2}}{1 + (K-2)z^{-1} + (1-K\beta)z^{-2}} \tag{2}$$

where we used $K = K_d K_w RT$, a normalized loop gain, and $\beta = 1 - T/RC$ which is always less than 1.

The input signal phase can be described as

$$\theta_i(n) = \theta_R(n) + \theta_N(n) = \theta_S + n\theta_T + \theta_N(n) \tag{3}$$

where $\theta_R(n)$ is the reference signal phase at time nT; θ_S is the phase offset; $n\theta_T$ is the frequency offset; and $\theta_N(n)$ is the phase jitter at time nT.

Suppose the phase jitter is a zero-mean white Gaussian process, i.e., $\theta_N(n) \sim \mathcal{N}(0, \sigma_N^2)$. From the transfer function (2), the output phase of the PLL in the discrete-time domain is given by

$$\begin{aligned}\theta_p(n+1) = {} & (2-K)\theta_p(n) + (K\beta - 1)\theta_p(n-1) \\ & + K\theta_i(n) - K\beta\theta_i(n-1).\end{aligned} \tag{4}$$

If we define the prediction error θ_d as a deviation of the output phase θ_p from the true phase θ_R, θ_d can be expressed as

[1]The model in [31] applied the impulse invariant transformation to $\Theta_p(s)/[\Theta_i(s) - \Theta_p(s)]$.

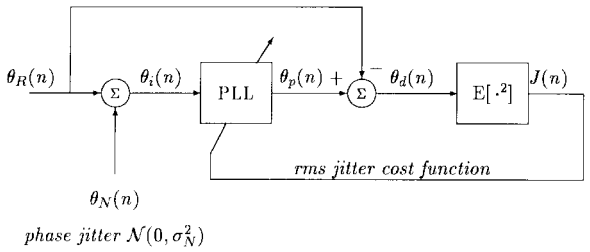


Fig. 2. Block diagram of optimizing scheme for obtaining the optimum gear-shifting sequence of PLL loop gain.

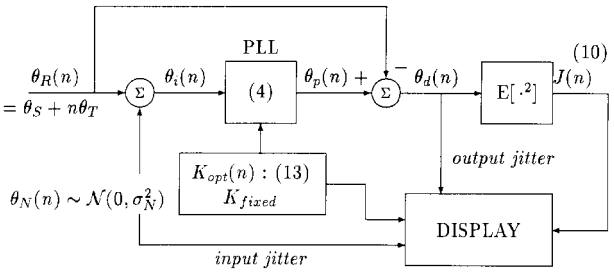


Fig. 3. Simulation setup for the behavioral model of the optimum gear-shifting CP-PLL. Numbers refer to equations.

follows:

$$\theta_d(n+1) \equiv \theta_p(n+1) - \theta_R(n+1) \tag{5}$$
$$= (2-K)\,\theta_d(n) + (K\beta - 1)\,\theta_d(n-1) + K\theta_N(n) - K\beta\theta_N(n-1). \tag{6}$$

Define $J(n)$, the cost function, as

$$J(n) \equiv E\big[\theta_d^2(n)\big]. \tag{7}$$

The optimizing scheme for minimizing a cost function is shown in Fig. 2. The minimum rms phase jitter at each time step can be obtained by minimizing the cost function $J(n)$, i.e., finding K satisfying $\partial J(n)/\partial K = 0$, since we intend to optimize PLL jitter performance with varying parameter K (loop gain). Solving (7) gives the following recurrence equation:

$$J(n+1) = (2-K)^2 J(n) + (K\beta-1)^2 J(n-1) + K^2(1+\beta^2)\sigma_N^2 + 2(2-K)(K\beta-1) \times E[\theta_d(n)\theta_d(n-1)] - 2K\beta\,(2-K)K_p\sigma_N^2 \tag{8}$$

where we used the orthogonalities

$$\begin{cases} E[(\theta_p(n) - \theta_R(n))\theta_N(n)] & = 0 \\ E[(\theta_p(n-1) - \theta_R(n-1))\theta_N(n)] & = 0 \\ E[(\theta_p(n-1) - \theta_R(n-1))\theta_N(n-1)] & = 0 \end{cases} \tag{9}$$

and K_p denotes a previous time step value of K.

The expectation term to be evaluated in (8) is an autocorrelation function of the prediction error θ_d at time instance n. The MSE $J(n+1)$ in (8) may be rewritten as

$$J(n+1) = (2-K)^2 J(n) + (K\beta-1)^2 J(n-1) + K^2(1+\beta^2)\sigma_N^2 + 2(2-K)(K\beta-1)C_p(n) - 2K\beta(2-K)K_p\sigma_N^2 \tag{10}$$

where we define $C_p(n)$ for notational convenience as

$$C_p(n) \equiv E[\theta_d(n)\theta_d(n-1)]. \tag{11}$$

Since $J(n+1)$ is a quadratic function of K, the optimal K minimizing this cost function exists and satisfies $\partial J(n+1)/\partial K = 0$, that is,

$$\frac{\partial J(n+1)}{\partial K} = -2(2-K)J(n) + 2\beta(\beta K - 1)J(n-1) + 2K(1+\beta^2)\sigma_N^2 + (4\beta + 2 - 4\beta K)C_p(n) - 4\beta K_p(1-K)\,\sigma_N^2 = 0. \tag{12}$$

TABLE I
ALGORITHM FOR COMPUTING AN OPTIMUM GEAR-SHIFTING SEQUENCE

(zero-phase start operation)

1. Initialization:
   Given T, R, and C.
   Compute $\beta = 1 - \frac{T}{RC}$.
   Set $\theta_p(n)$, $J(n)$, $n = [-1, 0, 1, 2]$.
   Set $C_p(n)$, n=[0,1,2], K_1, and K_2.
   Set $K_2 = \frac{4}{3}$.
   Set $n = 2$, *iter*.
2. Compute K_{n+1} from (13).
3. Compute $J(n+1)$, $C_p(n+1)$ from (10), (14).
4. Compute the output phase $\theta_p(n+1)$ from (4).
5. Set $n \Rightarrow n+1$.
6. If $n < iter$, go to 2.
7. Check K_n, $J(n)$, and $\theta_p(n)$ with $\theta_i(n)$.

Hence the optimum gear-shifting K minimizing $J(\cdot)$ at the time instance $n+1$ can be written as

$$K_{n+1} = \frac{2J(n) + \beta J(n-1) - (2\beta+1)\,C_p(n) + 2\beta K_n\,\sigma_N^2}{J(n) + \beta^2 J(n-1) - 2\beta\,C_p(n) + (1 + 2\beta K_n + \beta^2)\,\sigma_N^2}. \tag{13}$$

Now, consider $C_p(n+1)$. Substituting (6) into (11) and the orthogonalities in (9) yield

$$C_p(n+1) = E[\theta_d(n+1)\,\theta_d(n)] = E\{[(2-K_{n+1})\theta_d(n) + (\beta K_{n+1} - 1)\theta_d(n-1) + K_{n+1}\theta_N(n) - \beta K_{n+1}\theta_N(n-1)]\theta_d(n)\} = (2-K_{n+1})J(n) + (\beta K_{n+1} - 1)C_p(n) - \beta K_n K_{n+1}\sigma_N^2. \tag{14}$$

In practice, it is difficult to evaluate the optimum gain sequence in (13), since in most real applications we do not know the input jitter variance σ_N^2 and the reference input phase θ_R. To obtain practically useful expression of K_n, we consider the following ZPS operation. Since two initial conditions are required to solve the second-order difference equation in (10), we assume the ZPS operations at $n = -1$ and 0, i.e., $\theta_p(-1) = \theta_i(-1)$ and $\theta_p(0) = \theta_i(0)$ by aligning the VCO output phase with the PLL input phase precisely. It means that we should compare and align VCO output phase with the input phase at initial consecutive time steps $n = -1$ and 0. Then, we have

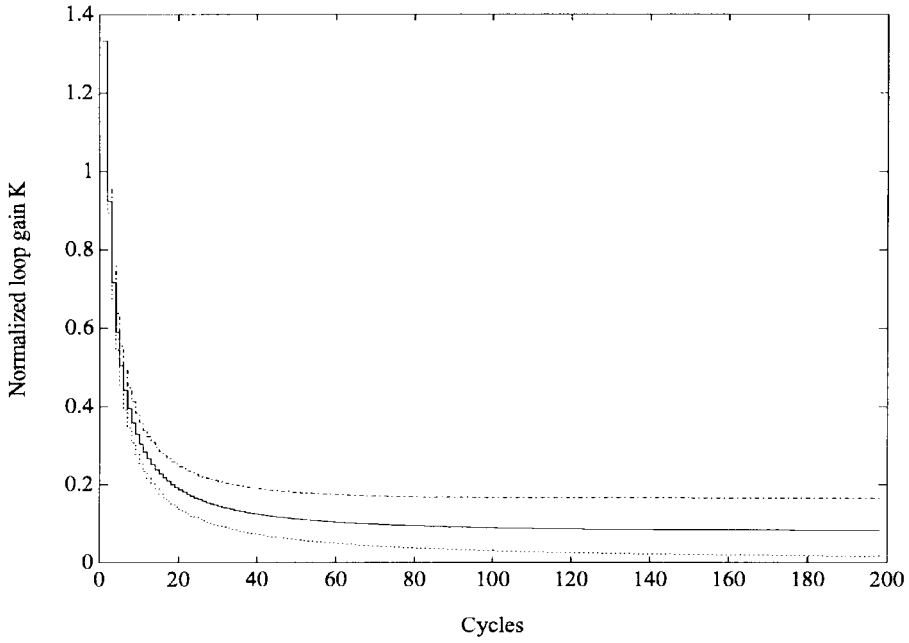


Fig. 4. Optimum gain sequences with various β i.e., 0.9, $(- \cdot - \cdot -)$, 0.95 (—), and 0.9986 $(--)$.

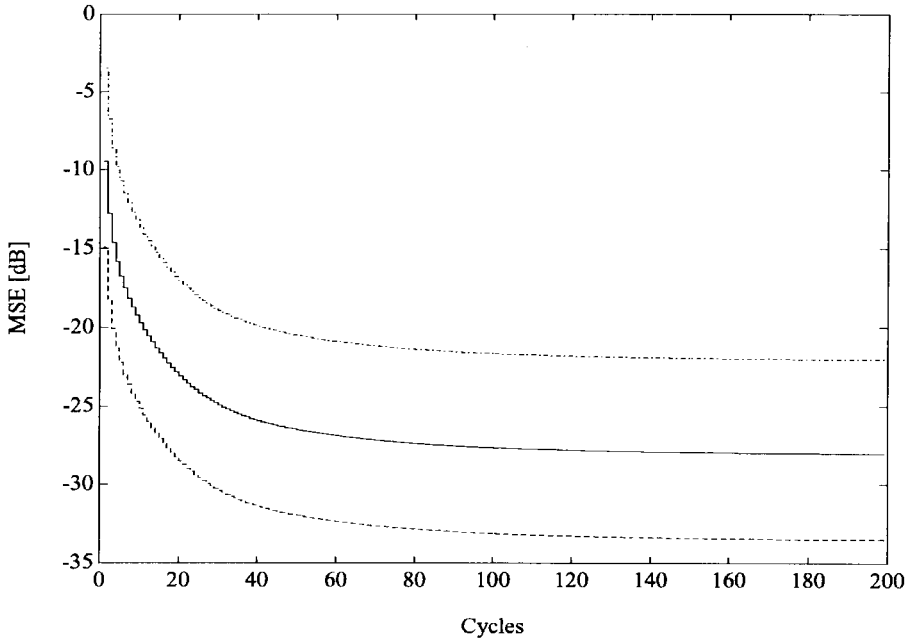


Fig. 5. MSE using optimum K_n sequence with several noise variances $\sigma_N^2 = 0.3^2$ $(- \cdot - \cdot -)$, 0.15^2 (—) and 0.08^2 $(--)$, where $\beta = 0.95$.

$\theta_d(-1) = \theta_p(-1) - \theta_R(-1) = \theta_i(-1) - \theta_R(-1) = \theta_N(-1)$, and $\theta_d(0) = \theta_p(0) - \theta_R(0) = \theta_i(0) - \theta_R(0) = \theta_N(0)$. Thus

$$J(-1) = E\left[\theta_d^2(-1)\right] = E\left[\theta_N^2(-1)\right] = \sigma_N^2$$
$$J(0) = E\left[\theta_d^2(0)\right] = E\left[\theta_N^2(0)\right] = \sigma_N^2$$
$$C_p(0) = E[\theta_d(0)\theta_d(-1)] = E[\theta_N(0)\theta_N(-1)] = 0.$$

$J(n), C_p(n), \theta_p(n)$ are as follows when $n = 1, 2$.

$$\begin{aligned} J(1) &= E\left[\theta_d^2(1)\right] \\ &= E\{[(2-K_1)\theta_d(0) + (K_1\beta - 1)\theta_d(-1) \\ &\quad + K_1\theta_N(0) - K_1\beta\theta_N(-1)]^2\} \\ &= E\{[2\theta_N(0) - \theta_N(-1)]^2\} = 5\sigma_N^2 \\ C_p(1) &= E[\theta_d(1)\theta_d(0)] = 2\sigma_N^2 \\ \theta_p(1) &= 2\theta_i(0) - \theta_i(-1) \\ J(2) &= E\left[\theta_d^2(2)\right] \\ &= E\{[(2-K_2)\theta_d(1) + (K_2\beta - 1)\theta_d(0) \\ &\quad + K_2\theta_N(1) - K_2\beta\theta_N(0)]^2\} \\ &= E\{[K_2\theta_N(1) + (3-2K_2)\theta_N(0) \\ &\quad - (2-K_2)\theta_N(-1)]^2\} \\ &= \left(6K_2^2 - 16K_2 + 13\right)\sigma_N^2. \end{aligned}$$

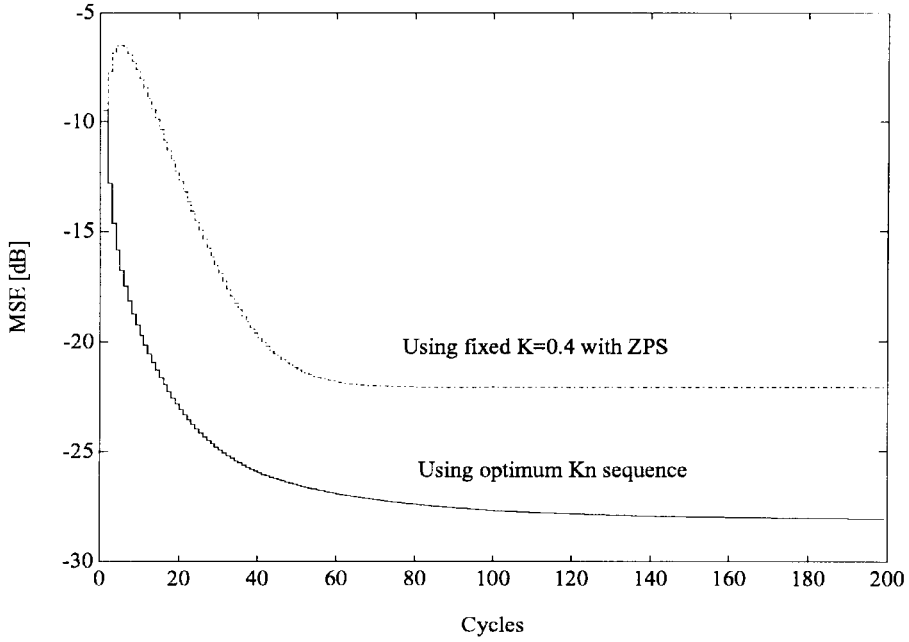


Fig. 6. MSE comparison between the CP-PLL's with the optimum K_n sequence and a fixed value of K (= 0.4) under conditions of approximately equal convergence rates. Here $\sigma_N^2 = 0.15^2$ and $\beta = 0.95$.

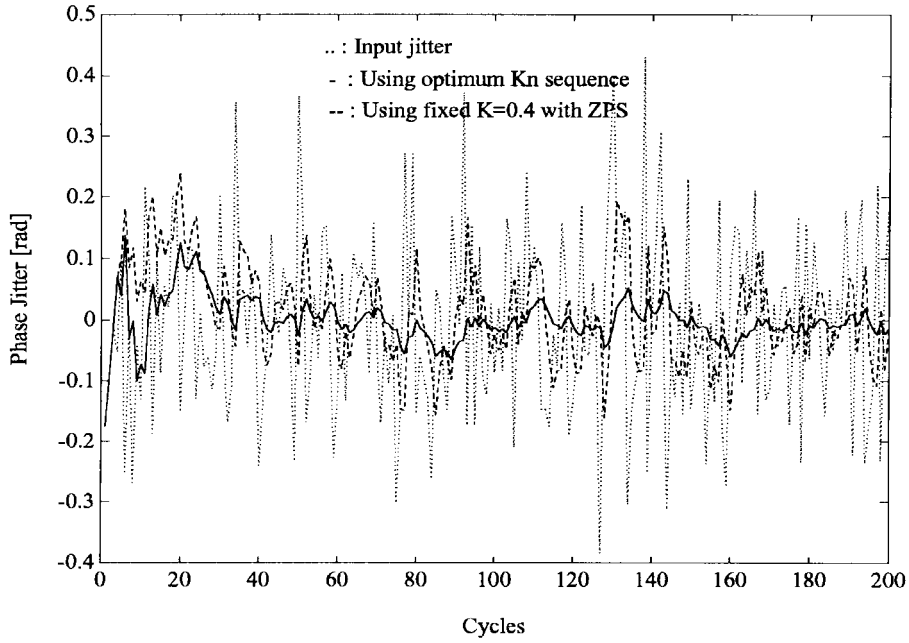


Fig. 7. Real-time phase acquisition using the optimum K_n sequence and a fixed value of K (=0.4) where σ_N^2 and β are 0.15^2 and 0.95, respectively.

Since K_2 minimizing $J(2)$ can be obtained by $\partial J(2)/\partial K_2 = 12K_2 - 16 = 0$, K_2 is 4/3 independent of σ_N^2, and $J_{\min}(2)$ is $(7/3)\sigma_N^2$. $C_p(2)$ and $\theta_p(2)$ are

$$\begin{aligned} C_p(2) &= E[\theta_d(2)\theta_d(1)] \\ &= E\{[K_2\theta_N(1) + (3-2K_2)\theta_N(0) \\ &\quad - (2-K_2)\theta_N(-1)](2\theta_N(0) - \theta_N(-1))\} \\ &= E\{2(3-2K_2)\theta_N^2(0) + (2-K_2)\theta_N^2(-1)\} \\ &= (8-5K_2)\sigma_N^2 = \frac{4}{3}\sigma_N^2 \end{aligned}$$

$$\begin{aligned} \theta_p(2) &= (2-K_2)\theta_p(1) + (K_2\beta - 1)\theta_p(0) \\ &\quad + K_2\theta_i(1) - K_2\beta\theta_i(0) \\ &= K_2\theta_i(1) + (3-2K_2)\theta_i(0) - (2-K_2)\theta_i(-1). \end{aligned}$$

Now, as summarized in Table I, the calculation of K_n at $n = 3, 4, \cdots$ can be performed using (4), (10), (13), and (14), under the initial conditions. From (10) and (14), it is not difficult to see that under the ZPS assumption, both $J(n)$ and $C_p(n)$ are multiples of σ_N^2 for all n. In addition, they are independent of θ_S and θ_T. These facts indicate that for any n, K_n in (13) is *independent* of σ_N^2 and depends *only* on β under the ZPS

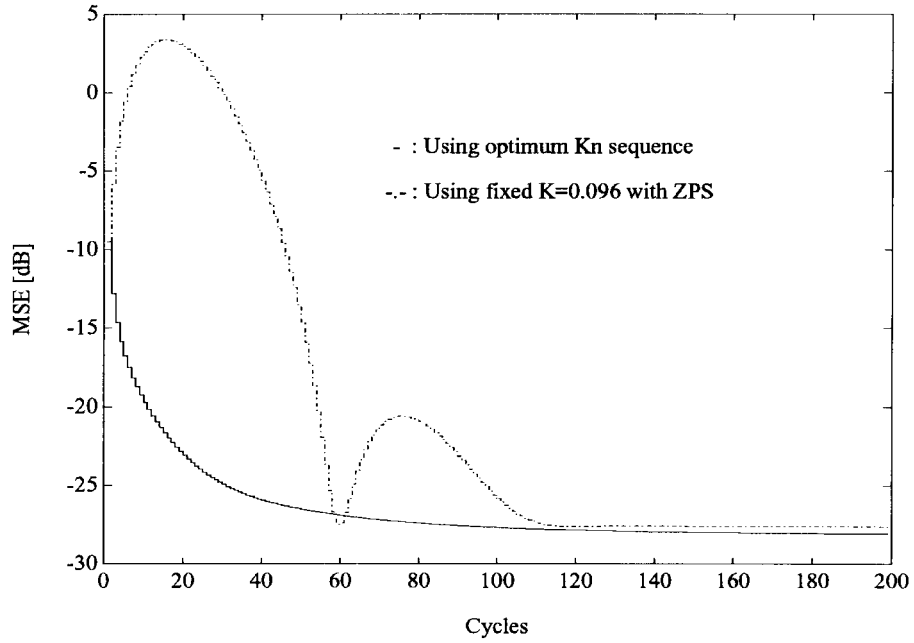


Fig. 8. MSE comparison between the CP-PLL's with the optimum K_n sequence and a fixed value of K (= 0.096) under conditions of approximately equal MSE in the steady state. Here $\sigma_N^2 = 0.15^2$ and $\beta = 0.95$.

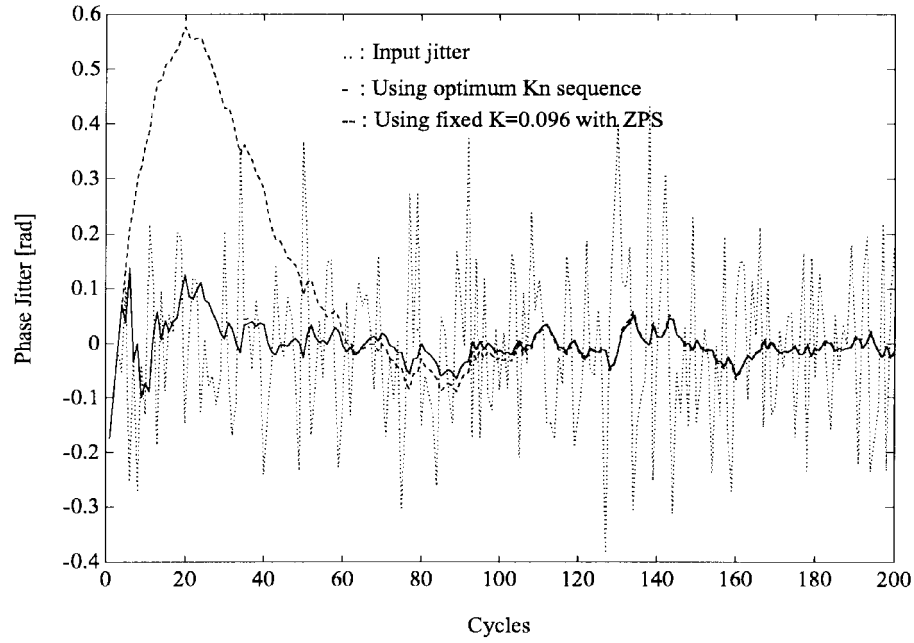


Fig. 9. Real-time phase acquisition using the optimum K_n sequence and a fixed value of K (=0.096) where σ_N^2 and β are 0.15^2 and 0.95, respectively.

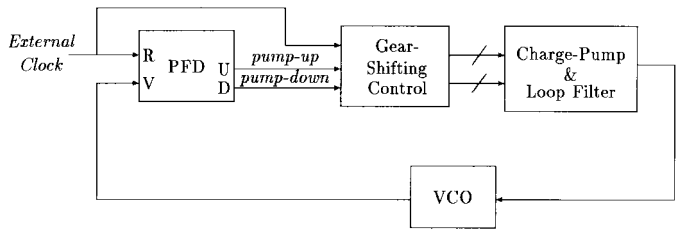


Fig. 10. Block diagram of a gear-shifting CP-PLL.

condition. Therefore, once β (or equivalently R, C, and T) is given, the K_n sequence can be evaluated and used for any input phase.

Next we show that the optimal K_n sequence can also be obtained under somewhat different initial condition. Specifically, we apply a ZPS condition only to the time $n = 0$ and set $\theta_p(-1) = 0$, then $\theta_d(-1) = \theta_p(-1) - \theta_R(-1) = \theta_T - \theta_S$, and

$$\begin{aligned} J(-1) &= E\left[\theta_d^2(-1)\right] = E[(\theta_T - \theta_S)^2] = (\theta_T - \theta_S)^2 \\ J(0) &= E\left[\theta_d^2(0)\right] = E\left[\theta_N^2(0)\right] = \sigma_N^2 \\ C_p(0) &= E[\theta_d(0)\theta_d(-1)] = E[\theta_N(0)(\theta_T - \theta_S)] = 0 \\ J(1) &= E\left[\theta_d^2(1)\right] = E\{[2\theta_N(0) - K_1\beta\theta_N(-1) \\ &\quad + (K_1\beta - 1)(\theta_T - \theta_S)]^2\} \\ &= 4\sigma_N^2 + K_1^2\beta^2\sigma_N^2 + (K_1\beta - 1)^2(\theta_T - \theta_S)^2. \end{aligned}$$

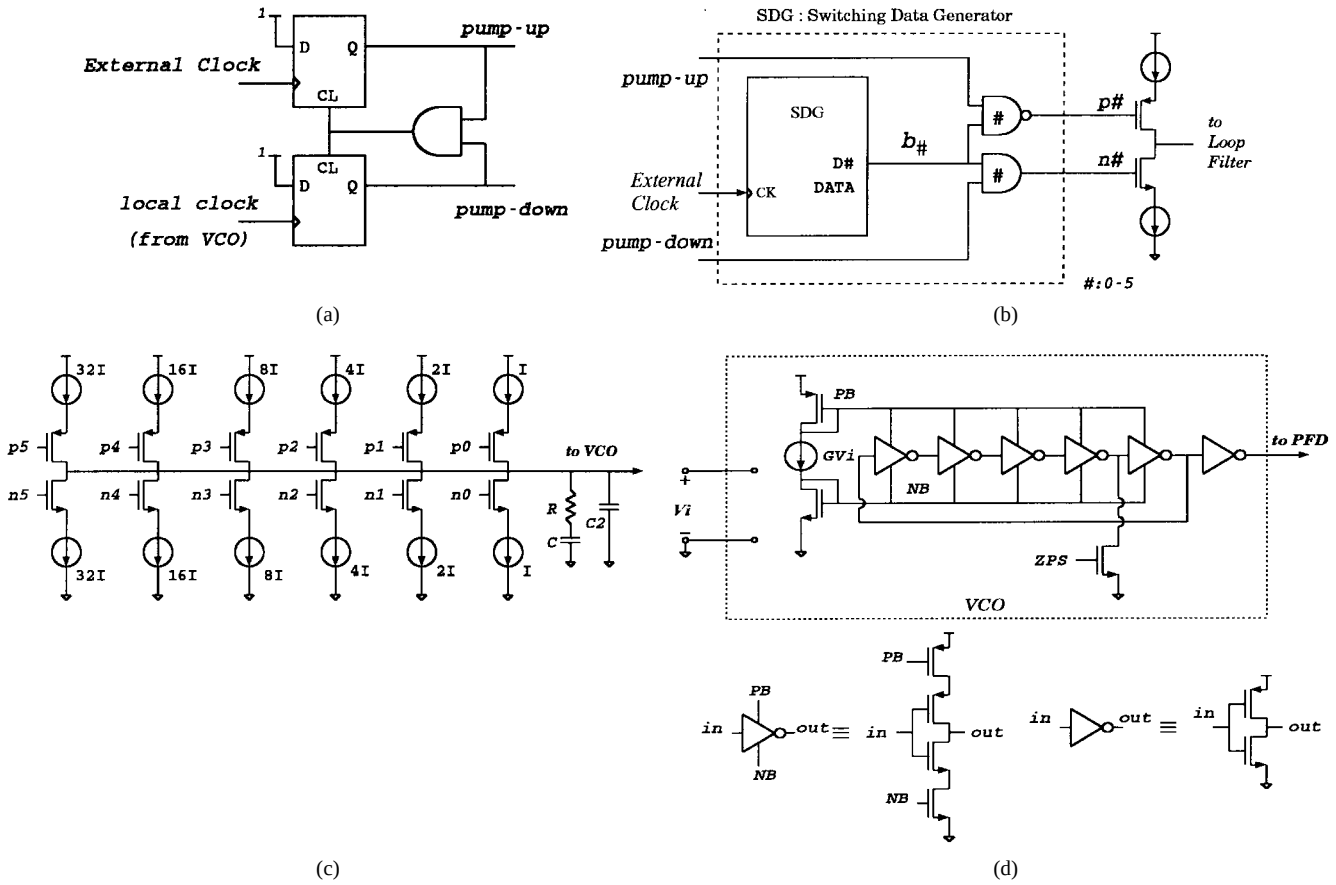


Fig. 11. Simplified schematics of the basic circuit elements. (a) PFD. (b) Gear-shifting control. (c) Charge-pump and loop filter, here $I = I_{\min}$. (d) VCO.

K_1 minimizing $J(1)$ is

$$K_1 = \frac{(\theta_T - \theta_S)^2}{\beta[(\theta_T - \theta_S)^2 + \sigma_N^2]}. \tag{15}$$

Since σ_N^2 is smaller than $(\theta_T - \theta_S)^2$ in general, K_1 may be approximated by $1/\beta$. Therefore $J(1) \simeq 5\sigma_N^2$, and the subsequent K_n values are the same as those obtained under the double ZPS condition.

B. Behavioral Simulations

The simulation setup for the behavioral model of the optimum gear-shifting CP-PLL is shown in Fig. 3. K_n is calculated according to the procedure in Table I and the results are shown in Fig. 4 for several values of β. As expected, K_n decreases monotonically. Note that the K_n sequence decreases to a lower value as RC time constant of the loop filter increases.

Behavioral simulations have been performed for several values of θ_S, θ_T, and σ_N^2, which indeed showed that the MSE $J(n)$ does not depend on θ_S and θ_T. Some MSE values are shown in Fig. 5.

Next we compare the performance of CP-PLL's having fixed gain K and time varying optimal gain K_n. We first consider the CP-PLL with $K = 0.4$ whose convergence rate is comparable to that with the time varying K_n. Figs. 6 and 7 show the resulting MSE values and the phase acquisition characteristics, respectively. It is seen that the optimal K_n sequence caused smaller MSE values (about 6 dB) and smaller phase jitter as compared with the case of $K = 0.4$. Now we consider another fixed gain, $K = 0.096$ whose steady state MSE value is similar to that of the optimal sequence. For this case, the MSE and the phase acquisition characteristics are shown in Figs. 8 and 9. As expected, the fixed gain $K = 0.096$ caused slower convergence.

III. PLL Circuit Design

In this section, the optimum phase-acquisition algorithm is applied to the design of a CP-PLL and the performance of the designed CP-PLL is verified through simulation. The algorithm makes it possible to achieve both the fast locking and the low jitter CP-PLL by setting the CP-PLL loop gain to the values of the optimum gear-shifting sequence K_n. The loop gain to be varied is a product of the PFD gain K_d, the VCO gain K_w, the loop filter resistor R, and period T. Since it is not easy to change the passive component R and the VCO gain K_w, we shall change the PFD gain $K_d\,(=I_p(n)/2\pi)$ to adjust the loop gain. For the optimum gear-shifting sequence K_n, the optimum charge-pump current sequence is given by

$$I_p(n) = \frac{2\pi K_n}{K_w R T}. \tag{16}$$

The charge-pump current $I_p(n)$ can be generated by using multiple current sources. In our CP-PLL circuit, we employ six pairs of current sources and generate 64 distinct $I_p(n)$ values which are integer multiples of a current value $I_{\min}$ [refer to

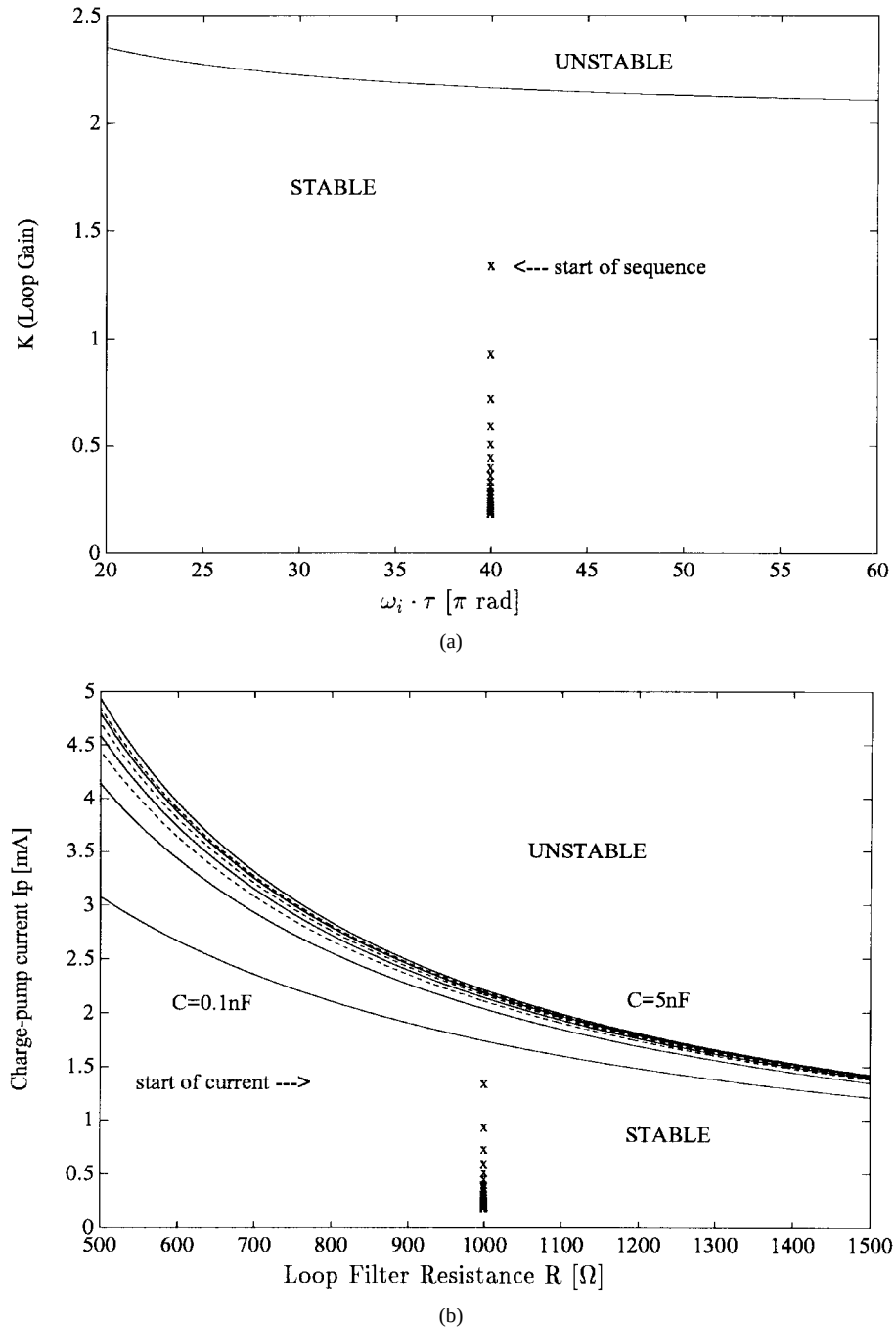


Fig. 12. Stability limit when $t_d = 0.1\tau = 0.1 \cdot RC$ where $R = 1$ kΩ and $C = 1$ nF. (a) Stable region of K values and locations of gear-shifting sequence. (b) Stable region of current and locations of values of gear-shifting current. From the top, the cases for $C = 5$, 2, 1.5, 1, 0.7, 0.5, 0.3, and 0.1 nF, respectively. $R = 1$ kΩ is used for $I_p(n)$.

Fig. 11(c)]. Here $I_{\min} = I_{\max}/63$ and $I_{\max}$ corresponds to the largest K_n value which is 4/3. In our design, we set $K_w = 2\pi \cdot$ 20 MHz/V, $R = 1$ kΩ, $C = 1$ nF, and $T = 50$ ns; the values of $I_{\min}$ and $I_{\max}$ are 21 and 1323 μA, respectively. The initial current value is equal to $I_{\max}$ and the final current value after 78 cycles is 82 μA. The charge-pump current value $I_p(n)$ obtained from (16) should be quantized to one of the 64 values. If we denote the quantized current by $\hat{I}_p(n)$, then $\hat{I}_p(n)$ can be expressed as $\hat{I}_p(n) = \sum_{i=0}^{5} b_i 2^i I_{\min}$ where b_i is either 0 or 1 and $b_5 b_4 \cdots b_1 b_0$ is the radix two representation of a positive integer between 0 and 63. The switches of charge-pump current sources will be controlled depending on the b_i values.

A. Gear-Shifting Charge-Pump PLL Circuit

Fig. 10 shows the proposed CP-PLL system. It has a gear-shifting control block between the PFD and the charge-pump circuit. The details of these blocks are shown in Fig. 11. A well-known three-state PFD, shown in Fig. 11(a), is used for phase-frequency detection with a linear range of $\pm 2\pi$ [32]. Its outputs are *pump-up* and *pump-down* signals. When the rising edge of the external clock leads the rising edge of the VCO

output, *pump-up* is activated to a high-level until the rising edge of the VCO output arrives. Similarly, *pump-down* is activated when the VCO output leads the external clock. Both *pump-up* and *pump-down* are deactivated to a low level when the loop is in a perfectly locked state. *Pump-up* and *pump-down* are connected to the gear-shifting control circuit shown in Fig. 11(b), which controls the switching of charge-pump current to generate $\hat{I}_p(n)$ according to b_i's $(i = 0{\sim}5)$ stored in memory. The SDG (Switching Data Generator) is composed of the memory and some control logics. The b_i's are converted into active-low and active-high signals through NAND and AND gates, respectively, for PMOS and NMOS switch control. The SDG output is synchronized by the external clock input of the PFD. All logics in the PFD and the gear-shifting control blocks are programmed with HSPICE behavioral modeling using voltage controlled current sources, called G elements. The G elements are used to reduce simulation time.

The charge-pump circuit shown in Fig. 11(c) comprises a set of current sources whose values are given by $2^n I_{\min}$ for $n = 0, \cdots, 5$. By summing these currents, any current value from $I_{\min}$ ampere to $I_{\max}$ ampere can be generated. We employ equal size NMOS switches, and equal size PMOS switches. The loop filter is a simple passive RC low-pass filter. The capacitor C_2 ($C_2 = 5$ pF) which is in parallel with the RC impedance was deliberately added to mitigate the ripple [6].

The VCO is a current-controlled ring oscillator. Five delay cells are connected in series to make the required delay and are buffered with an inverter for signal conditioning. The input of the last stage of the ring oscillator is connected to the ground level through the NMOS switch to perform the ZPS operation. By deactivating the ZPS control input when the rising edge of the external clock is arrived, the VCO output can be synchronized to the external clock.

A lock detector which is not shown explicitly in Fig. 10 may be located externally. If the input goes out of the locking range, an external locking control circuit may stop the CP-PLL and restart the acquisition process.

B. Stability of a Gear-Shifting Charge-Pump PLL

A simplified stability analysis in [6] for the second-order CP-PLL was extended in [33], which gives the same results as in [9] if the logic delay time $t_d = 0$. When we include the effect of logic delay in the simplified analysis of the second-order loop filter in the z-domain, the stable operating conditions for K_n and I_p are given by

$$K_n < \frac{2}{\left[\frac{\pi}{\omega_i \tau} + 1 - \frac{t_d}{\tau}\right]}, \quad I_p < \frac{\omega_i}{K_o R \pi \left[\frac{\pi}{\omega_i \tau} + 1 - \frac{t_d}{\tau}\right]}$$

where K_o = VCO gain in MHz/volt; ω_i = input frequency in rad/sec; and $\tau = RC$. The right-hand side terms in the above inequalities are the stability limits. The stability limit for a loop gain K of the PLL is shown in Fig. 12(a) against $\omega_i \tau$ in πrad using the values $K_o = 20$ MHz/volt, $R = 500{\sim}1500\ \Omega$, $t_d = 0.1\tau$, $C = 1$ nF, and $\omega_i = 2\pi \cdot 20$ M rad. The optimum gear-shifting sequence K_n is also shown for a stability check, and only the first 21 values of K_n are plotted since the sequence shows a monotonic decreasing trend into the more stable region. The stability limit for charge-pump current I_p is shown in Fig. 12(b) using the same values but various capacitors ranging from 0.1 to 5 nF. The first 21 values of optimum gear-shifting current $I_p(n)$ with $R = 1$ kΩ are shown together. As shown in Fig. 12, all the sequences K_n and $I_p(n)$ are within the stable region. In addition to the above conditions, we observed that the condition $z = \frac{\tau - t_d}{T + \tau + t_d} > 0$ in [33] is also met based on the z-domain analysis of transfer functions.

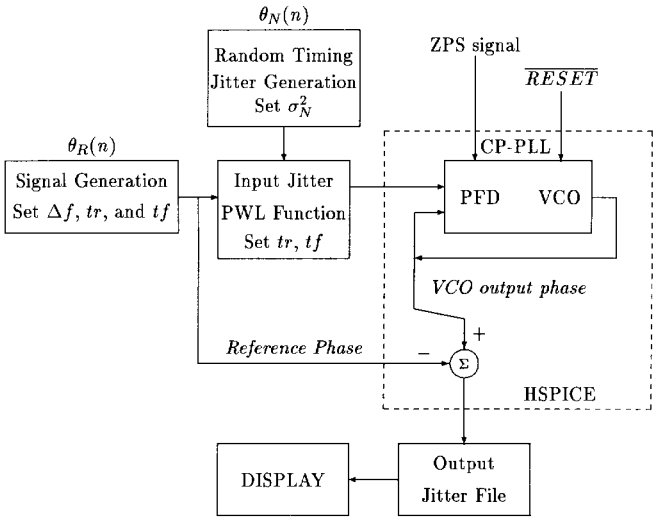
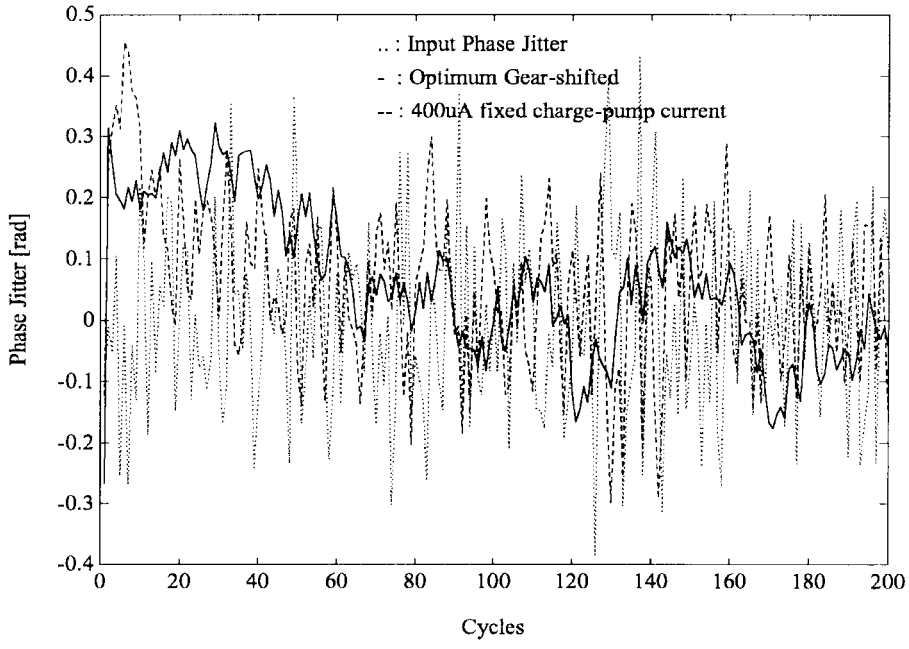


Fig. 13. Simulation setup for the circuit-level model of the optimum gear-shifting CP-PLL. Δf, tr, and tf denote the frequency offset, the rising time, and the falling time, respectively.

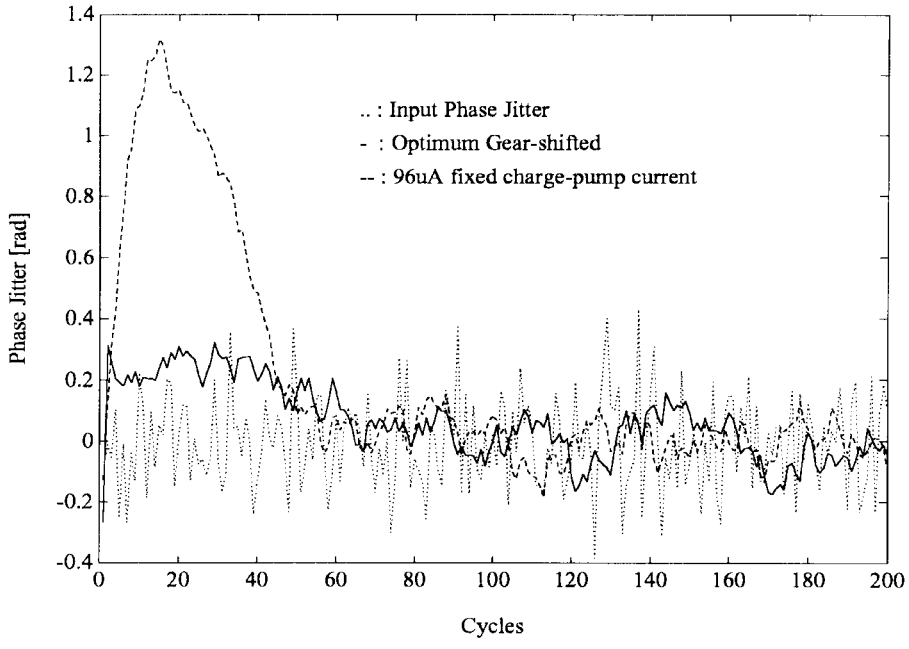
C. Circuit Simulations

The simulation setup for the circuit-level model of the optimum gear-shifting CP-PLL is shown in Fig. 13. An external jittered clock having some frequency offset should be fed to the input of the PFD. Since there is no direct method or function for simulating a jitter characteristic of CP-PLL in HSPICE, a C-program generating an input clock file having the modulated clock edges with random Gaussian phase jitter has been written. Signal generation block generates $\theta_R(n)$. Input jitter block adds the random phase $\theta_N(n)$ generated by the random timing jitter generation block to $\theta_R(n)$. The rising and falling times of the external clock input were intentionally made similar to those of the VCO output. The jittered input clock file is composed of PWL (Piecewise Linear Source) waveform functions. Output phase jitter is measured by subtracting each reference phase from the VCO output phase. Additionally, a ZPS operation control signal and an initial PLL reset signal are used. R and C are 1 kΩ and 1 nF, respectively.

The simulations of the CP-PLL were performed using the HSPICE circuit simulator from Metasoft with 2 μm design parameters, and the results are shown in Fig. 14. In Fig. 14(a), three curves are shown representing the output phase jitter for a fixed charge-pump current 400 μA, the output phase jitter for a gear-shifting charge-pump current, and the input phase jitter for reference. Fig. 14(b) shows those curves in the case of fixed charge-pump current 96 μA. All CP-PLL's



(a)



(b)

Fig. 14. Simulation results with ZPS. (a) Phase jitter outputs for $I_p = 400$ μA and $I_p(n)$. (b) Phase jitter outputs for $I_p = 96$ μA and $I_p(n)$.

employ the ZPS operation. In this simulation, we use the PFD input with one percent frequency offset and the input jitter variance $\sigma_N^2 = 0.15^2$. The CP-PLL with 400 μA charge-pump current exhibits a comparable acquisition speed, but caused much larger phase jitter than the gear-shifting CP-PLL. The CP-PLL with 96 μA caused comparable output jitter in the steady-state, but requires much longer convergence time. It is interesting to compare the results in Fig. 14(a) with those in Fig. 7, because $I_p = 400$ μA corresponds to the fixed gain $K = 0.4$. As expected, the result in Fig. 14(a) exhibit larger variations. This is mainly because of the nonlinearities of the circuit elements. Although these figures show somewhat different phase jitter curves, they lead to the same conclusion: the gear-shifting CP-PLL caused smaller phase jitter variance than the fixed CP-PLL.

The acquisition speeds of the CP-PLL under various conditions were investigated for a statistical performance comparison. Histograms of the acquisition speed are plotted in Fig. 15, where we define the acquisition speed as the time required for an output phase jitter to fall within 5% of the input period. We have run simulations with 49 different jitter patterns for each cases. As shown in Fig. 15, the acquisition speed for the optimum gear-shifting CP-PLL falls within about 20 cycles and the optimum gear-shifting CP-PLL outperforms

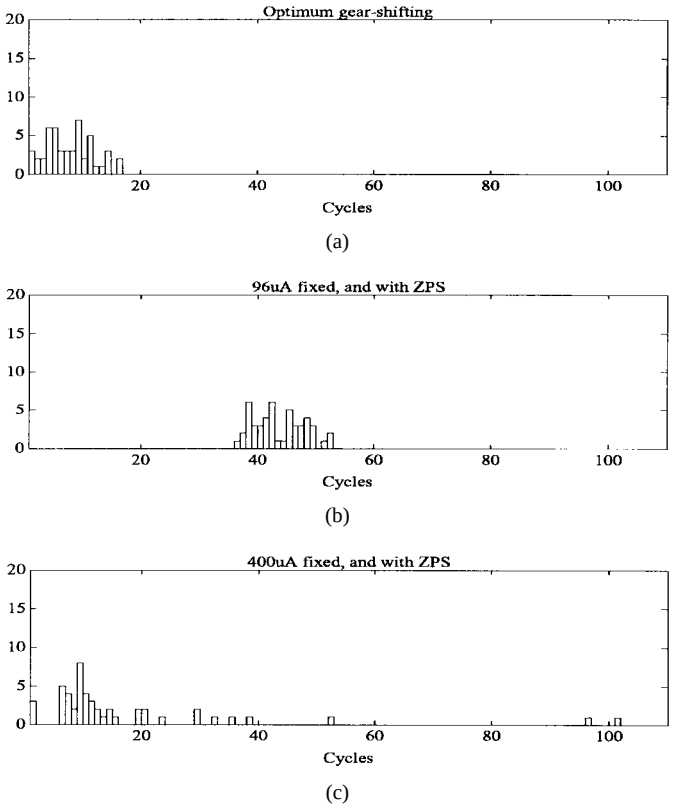


Fig. 15. Histograms illustrating the acquisition speed of the CP-PLL's. The horizontal-axis represents the acquisition speed in cycles, and the vertical-axis is the number of the jitter patterns for which the acquisition is achieved.

the conventional CP-PLL. Finally, in our simulation, we operated the optimum gear-shifting CP-PLL without the ZPS initialization. In this case, some performance degradation was observed but the gear-shifting CP-PLL was still effective for acquisition and outperformed the CP-PLL with fixed gain.

IV. Conclusion

A new optimum phase-acquisition algorithm, which we label the gear-shifting algorithm, was presented for a CP-PLL. The optimum gear-shifting sequence was obtained by solving a set of recursive difference equations under the ZPS assumption. Both behavioral simulation and circuit-level simulation results showed that this algorithm achieved both fast acquisition at the beginning and substantial output jitter reduction in the steady-state. A procedure for implementing the optimum gear-shifting algorithm on the CP-PLL circuit was described, and the performance of the algorithm was verified through the HSPICE circuit simulation. The design method developed here may be applicable to clock synchronizer implementation, as well as to other applications requiring very short initial preamble periods. The optimum gear-shifting CP-PLL can be fully integrated in a single chip with minor increase in hardware complexity as compared with the conventional CP-PLL.

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